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Application Number 10/665,521 Filing Date September 22, 2003 First Named Inventor Priyadarsan Patra et al. Art Unit 2825 **Examiner Name** Aneette M. Thompson (anticipated) Attorney Docket Number 2207/1254202

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Date	January 7, 2004		
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PATENT

DOCKET NO.: 2207/1254202

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant No.:

10/665,521

Applicants

Priyadarsan Patra et al.

Filed

September 22, 2003

TC/Art Unit :

2825 (Anticipated)

Examiner

Annette M. Thompson (Anticipated)

Docket No.

2207/1254202

Customer No:

23838

FOR

NOISE AND POWER OPTIMIZATION IN HIGH PERFORMANCE

CIRCUITS

Commissioner for Patents

P.O. Box 1450

Washington, D.C. 22313-1450

REQUEST FOR ISSUANCE OF A CORRECTED FILING RECEIPT

SIR:

Enclosed is a copy of the official Filing Receipt. Please correct the title to read NOISE AND POWER OPTIMIZATION IN HIGH PERFORMANCE CIRCUITS. The corrections are shown in blue ink on the enclosed copy of the Filing Receipt.

These corrections are apparent from the application papers and no fee is necessary. Issuance of a corrected filing receipt is respectfully requested.

Respectfully submitted,

Date: January 7, 2004

Shawn W. O'Dowd, Reg. No. 34,687

cc DT. 12/17/03



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10/665,521 09/22/2003

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23838 **KENYON & KENYON** 1500 K STREET, N.W., SUITE 700 JAN 0 7 2004

CONFIRMATION NO. 5814

FILING RECEIPT

OC000000011488757

Date Mailed: 12/15/2003

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Applicant(s)

Priyadarsan Patra, Portland, OR; Barbara Chappell, Portland, OR;

Domestic Priority data as claimed by applicant

This application is a CON of 09/964,803 09/28/2001

Foreign Applications

If Required, Foreign Filing License Granted: 12/12/2003

Projected Publication Date: 03/25/2004

Non-Publication Request: No

Early Publication Request: No

Title

Noise and Power

-power optimization of high performance circuits

Preliminary Class

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